REMARKS

The present response is intended to be fully responsive to all points of rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Claims 1-34 are pending in this case. Claims 29-30 have been rejected under 35 U.S.C. § 112, second paragraph. Claims 1-4, 6, 10-11, 13-14, 16-20, 23, 26-28, 31, 33-34 have been rejected under 35 U.S.C. § 103(a). Independent claims 1, 6, 9, 16, 28 and 31 and dependent claims 5, 9, 29-30 have been amended.

With respect to the Examiner's 35 U.S.C. § 103(a) rejections, Applicant has reviewed the cited art and respectfully submits that the art fails to disclose or suggest the Applicant's claimed invention. Therefore, Applicant respectfully traverses and requests favorable reconsideration.

Personal Interview

Applicant wishes to thank the Examiner for granting a personal interview on May 25, 2005. The interview participants included Examiner Jaison Joseph, SP Examiner Stephen Chin and Howard Zaretsky (Applicant's representative).

Missing Information Disclosure Statement

An Information Disclosure Statement was previously submitted by Applicant on April 29, 2002. An initialed copy of the PTO-1449 form was absent from the current Office Action mailed April 21, 2005. It is thus assumed that the original Information Disclosure Statement is missing from the file. A copy of the Information Disclosure Statement previously hand-filed including the date stamped transmittal sheet indicating the receipt of five references is enclosed with this Response. Applicant requests that the re-submission be considered received as of the original date, i.e. April 29, 2002.

Response to 35 U.S.C. § 112, Second Paragraph Rejections

The Examiner rejected claims 29-30 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Amended claims 29-30 now feature language which make it clear what the subject matter is that the Applicant regards as the invention. Applicant believes that amended claims 29-30 overcome the Examiner's rejection based on § 112, second paragraph grounds. The Examiner is respectfully requested to withdraw the § 112, second paragraph rejection.

Response to 35 U.S.C. § 103(a) Rejections

Regarding claims 1-4, 18-20, 23:

The Examiner rejected claims 1-4, 18-20, 23 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,707,844 ("Imaizumi et al.") in view of U.S. Patent No. 5,117,232 ("Cantwell").

While continuing to traverse the Examiner's rejections, Applicant, in order to expedite the prosecution, has chosen to clarify and emphasize the crucial distinctions between the present invention and the devices of the patents cited by the Examiner. Specifically, claim 1 has been amended to include a correlator for correlating an input signal with a code comprising a sample register adapted to store and output E input samples every chip period of an input sample stream clocked at an over sampling ratio of R times a nominal sampling clock rate, a single code register adapted to store and output a code value at the nominal sampling clock rate, a single multiplier coupled to the sample register and the code register, the multiplier adapted to multiply the output of the sample register with the output of the code register, a single adder adapted to add the output of the multiplier with a correlation sum output of the last stage of an M-stage integration result shift register and to produce an updated correlation sum therefrom, the integration results shift register adapted to store M correlation sums wherein updated correlation sums output of the adder are shifted into the integration results shift register at the over-sampling clock rate such that the over-sampling phase of the correlation sum at the output of the integration results shift register corresponds to the correlation sum currently at the input to the adder and wherein E, R and M are positive integers.

Imaizumi et al. teaches a synchronous circuit and a receiver in which a long code for use in communication systems can be determined within a short time, and the scale of the resulting circuit can be reduced. Upon receiving the input of a data stop signal from a control unit, a matched filter continues to hold the signal held at the time, performs a product sum operation of a spreading code successively inputted from a spreading code generator and the held signal, and successively outputs correlation signals in the synchronous circuit and the receiver.

Cantwell teaches an apparatus and method for pseudo-random noise (PN) code correlation in a GPS receiver employing sign and magnitude input weighting for each of the in-phase (I) and quadrature-phase (Q) samples of a received PN-code modulated carrier. A programmable R factor provides input A/D sample sign and magnitude weighting control of outside crossing samples for interference rejection of other RF signals interfering with the received PN-code modulated RF carrier. The R factor weighting determines if the A/D samples are from a linear or adaptive A/D converter. In-phase reference (IREF) signals and quadrature-phase reference (QREF) signals,

produced by an internally generated PN-code reference, are provided to a plurality of I and Q multi-Y-tap correlator/integrators for correlation with the I and Q samples. The apparatus correlates I and Q samples obtained from IF sampling or baseband sampling of the received PN-code modulated carrier.

It is submitted that the present invention is a reduced complexity correlator wherein a single multiplier and adder operate in conjunction with an integration results shift register. The integration results shift register is adapted to store a plurality of partial correlation sums, one for each input sample/code combination. The correlation sums are calculated over multitude symbol times wherein a correlation sum is maintained for each sample time within the symbol and for each code (in the case of multiple codes per sample). In operation, the clocking of the sample register, code register and integration results shift register is adjusted such that the correlation sum output of the integration results shift register corresponds to the correlation result presently being calculated. These features are neither taught nor suggested by the Imaizumi et al. or Cantwell references.

It is submitted that the combination of Imaizumi et al. and Cantwell would not result in the claimed invention. The combination suggested by the Examiner fails to teach or suggest all the limitations of each claim. The combination of Imaizumi et al. and Cantwell fails to teach a single multiplier, single adder and integration results shift register as taught by the present invention.

The Applicant respectfully traverses the rejection of claims 1-4, 18-20, 23 and submits that the presently claimed invention are patently distinct over Imaizumi et al. in view of Cantwell. It is believed that claims 1-4, 18-20, 23 overcome the Examiner's § 103(a) rejection based on the Imaizumi et al. and Cantwell references. The Examiner is respectfully requested to withdraw the rejection based on § 103(a).

Regarding claims 6, 10-11, 13-14, 28, 31:

The Examiner rejected claims 6, 10-11, 13-14, 28, 31 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,707,844 ("Imaizumi et al.") in view of U.S. Patent No. 5,117,232 ("Cantwell") and further in view of U.S. Patent No. 6,539,048 ("Hakala").

While continuing to traverse the Examiner's rejections, Applicant, in order to expedite the prosecution, has chosen to clarify and emphasize the crucial distinctions between the present invention and the devices of the patents cited by the Examiner. Specifically, representative claim 6 has been amended to include a correlator for correlating input samples with a plurality of codes comprising a sample register adapted to store and output input samples at a first clock rate, an N-stage circular code shift register adapted to store N code values and clocked at a second clock rate, a

single multiplier coupled to the sample register and the code shift register, the multiplier for multiplying input samples with the code value output of the last stage of the code shift register, wherein the code shift register is circularly shifted such that each input sample is sequentially multiplied by each of N codes, a single adder adapted to add the output of the multiplier with a correlation sum output of the last stage of an M-stage integration result shift register and to produce an updated correlation sum therefrom, the integration results shift register adapted to store M correlation sums wherein updated correlation sums output of the adder are shifted into the integration results shift register at the second clock rate such that the correlation sum at the output of the integration results shift register corresponds to that of the correlation sum currently at the input to the adder and wherein N and M are positive integers.

Hakala teaches a mobile station for receiving a spread spectrum, code division transmission from at least one transmitter, such as a base station. The mobile station contains a receiver for outputting data samples, and further contains a multi-tap ring matched filter. The ring matched filter is constructed to have first circuitry for storing an individual one of a received data sample into an individual one of a plurality storage registers such that a active data sample that has been stored for the longest period of time is overwritten with a most recently received data sample. The ring matched filter is further constructed to have second circuitry for serially shifting coefficient bits of at least one multi-bit spreading code relative to the storage registers for sequentially and simultaneously correlating the at least one multi-bit spreading code with a plurality of corresponding stored data samples, while significantly reducing power consumption by limiting state changes of flip-flops.

For the reasons stated hereinabove, it is submitted that the combination of Imaizumi et al., Cantwell and Hakala would not result in the claimed invention. The combination suggested by the Examiner fails to teach or suggest all the limitations of each claim. The combination of Imaizumi et al., Cantwell and Hakala fails to teach a single multiplier, single adder and integration results shift register as taught by the present invention.

The Applicant respectfully traverses the rejection of claims 6, 10-11, 13-14, 28, 31 and submits that the presently claimed invention are patently distinct over Imaizumi et al. in view of Cantwell in further view of Hakala. It is believed that claims 6, 10-11, 13-14, 28, 31 overcome the Examiner's § 103(a) rejection based on the Imaizumi et al., Cantwell and Hakala references. The Examiner is respectfully requested to withdraw the rejection based on § 103(a).

Regarding claims 16-17:

The Examiner rejected claims 16-17 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,005,889 ("Chung et al.") in view of U.S. Patent No. 6,707,844 ("Imaizumi et al."), U.S. Patent No. 5,117,232 ("Cantwell") and U.S. Patent No. 6,539,048 ("Hakala").

For the reasons stated hereinabove, it is submitted that the combination of Chung et al., Imaizumi et al., Cantwell and Hakala would not result in the claimed invention. The combination suggested by the Examiner fails to teach or suggest all the limitations of each claim. The combination of Chung et al., Imaizumi et al., Cantwell and Hakala fails to teach a single multiplier, single adder and integration results shift register as taught by the present invention.

The Applicant respectfully traverses the rejection of claims 16-17 and submits that the presently claimed invention are patently distinct over Chung et al. in view of Imaizumi et al., Cantwell and Hakala. It is believed that claims 16-17 overcome the Examiner's § 103(a) rejection based on the Chung et al., Imaizumi et al., Cantwell and Hakala references. The Examiner is respectfully requested to withdraw the rejection based on § 103(a).

Regarding claims 26-27, 33-34:

The Examiner rejected claims 26-27, 33-34 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,707,844 ("Imaizumi et al.") in view of U.S. Patent No. 5,117,232 ("Cantwell") and U.S. Patent No. 6,539,048 ("Hakala") and further in view of U.S. Patent No. 6,501,788 ("Wang et al.").

For the reasons stated hereinabove, it is submitted that the combination of Imaizumi et al., Cantwell, Hakala and Wang et al. would not result in the claimed invention. The combination suggested by the Examiner fails to teach or suggest all the limitations of each claim. The combination of Imaizumi et al., Cantwell, Hakala and Wang et al. fails to teach a single multiplier, single adder and integration results shift register as taught by the present invention.

The Applicant respectfully traverses the rejection of claims 26-27, 33-34 and submits that the presently claimed invention are patently distinct over Imaizumi et al. in view of Cantwell and Hakala and further in view of Wang et al. It is believed that claims 26-27, 33-34 overcome the Examiner's § 103(a) rejection based on the Imaizumi et al., Cantwell, Hakala and Wang et al. references. The Examiner is respectfully requested to withdraw the rejection based on § 103(a).

Correction of Typographical Errors

Amendments haven been made to correct grammatical and usage errors in the specification. No new matter has been added to the application by these amendments.

Conclusion

In view of the above amendments and remarks, it is respectfully submitted that independent claims 1, 6, 16, 28, 31 and hence dependent claims 2-5, 7-15, 17-27, 29-30, 32-34 are now in condition for allowance. Prompt notice of allowance is respectfully solicited.

In light of the Amendments and the arguments set forth above, Applicant earnestly believes that they are entitled to a letters patent, and respectively solicit the Examiner to expedite prosecution of this patent applications to issuance. Should the Examiner have any questions, the Examiner is encouraged to telephone the undersigned.

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Respectfully submitted,

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